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EXAMINER

TORRES, JOSEPH D

ART UNIT PAPER NUMBER

2133

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/870,955

Applicant(s)

HILLIGES, KLAUS-DIETER

Examiner

Joseph D. Torres

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-10 and 12-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-10 and 12-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. In view of the Amendment filed 12 July 2004, the Examiner withdraws the previous 35 USC § 112 rejection to claims 1, 2, 4-10 and 12-19 in the previous Office Action filed 09 April 2004.

Response to Arguments

2. Applicant's arguments with respect to claims 1, 2, 4-10 and 12-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 2, 4-10 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheung, David K. et al. (US 5461310 A, hereafter referred to as Cheung) in view of Le; Dai Minh (US 6353904 B1).

35 U.S.C. 103(a) rejection of claim 1.

Cheung teaches automated test equipment ATE (col. 1, lines 13-14, Cheung) comprising:

a plurality of per-pin testing units (See Figure 1 in Cheung), wherein each of said plurality of per-pin testing units has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test (DUT) having a plurality of DUT pins (Driver 26 and Comparator 28 in Figure 1 of Cheung are circuitry providing each of said plurality of per-pin testing units circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test),

and wherein, during a testing sequence, said DUT is defined as 1. a first DUT core that represents a first functional unit of said DUT and 2. a second DUT core that represents a second functional unit of said DUT (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different

grouping of pin slice circuits represent different core functional units within the circuit); means for assigning, during said testing sequence, a subset of said plurality of per-pin testing units to an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins (col. 2, lines 8-15 in Cheung teach that groups of Pin Slice Circuits are used to test different functional components giving an example whereby one 6 pin group is used for testing transistor-transistor logic, TTL, and another grouping of six pins is used for testing Emitter Coupled Logic, ECL, and another grouping comprising the 6 pin group for testing the TTL functional unit and the 6 pin group for testing the ECL functional unit is used to test the combined TTL-ECL functional unit; the Abstract in Cheung teaches that participate memory is a means for assigning groupings of Pin Slice Circuits; Note: the pin channels for a grouping comprise an ATE-port for the particular functional unit that is being tested, for example; the 6 pin group for testing the TTL functional unit is an ATE-port, the 6 pin group for testing the ECL functional unit is an ATE-port and the 12 pin group for testing the combined TTL-ECL functional unit is an ATE-port); and means for programming said ATE-port with a program for testing said first DUT core (col. 1, lines 13-37 of Cheung explicitly teach that the test system computer within an ATE stores programs for testing the DUT and the Abstract in Cheung explicitly teaches that the different groupings of pin slice circuits are programmed whereby pin slice circuits in the same group are programmed with the same test signals), wherein said program defines at least one of programming timing or a stimulus/response pattern (see Abstract; Note: a test signal is a stimulus/response pattern), and specifies a per-pin timing in terms of sets of available waveforms for each

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of said plurality of per-pin testing units assigned to said ATE-port (Claim 12 in Cheung teaches that Event Sequencer Memory 24 in figure 1 of Cheung stores a plurality of timing criteria for each pin, i.e., per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port), wherein each waveform represents a sequence of events of various types occurring at specified instances in time (Event Sequencer 24 in Figure 1 of Cheung teaches each waveform represents a sequence of events of various types occurring at specified instances in time), and wherein said program is independent of a program for testing said second DUT core (col. 2, lines 8-15 of Cheung explicitly teach "one grouping from the participate memory is used to program the data pattern in parallel to the dozen inputs, while two separate groupings are used to program the voltage levels for digital zeros and ones separately for the TTL inputs and the ECL inputs", hence Cheung teaches two different programs, a first test program for a first grouping and a second test program for second and third groupings).

However Cheung does not explicitly teach the specific use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification.

Le, in an analogous art, teaches use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification (Figure 2 and 4 in Le teaches a programming component that obtains a specification 270 in Figure 2 for testing a DUT core and prepares a program 460 in Figure 4 based on said specification 270). Note: col. 4, lines 23-33 in Cheung teach

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that various test programs are required to implement the design in Cheung, but does not teach the details to the test program generation. Le, on the other hand teaches test program generation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cheung with the teachings of Le by including use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification would have provided the opportunity to generate the test programs required in the Cheung patent.

35 U.S.C. 103(a) rejection of claim 2.

Cheung teaches means for switching connections between one or more of said plurality of per-pin testing units and one or more of said plurality of DUT pins (the Abstract in Cheung teaches that participate memory is a means for assigning groupings of Pin Slice Circuits, Note: the participate memory is a switching means for switching connections between one or more of said per-pin testing units and one or more of said DUT-pins), and means for controlling said switching in accordance with said assigning of said subset of said plurality of per-pin testing units (col. 5, lines 38-42 in Cheung, Note: the group select signal is a controlling means for controlling the switching of said

switching means in accordance with the assigning of said one or more of the per-pin testing units to said one or more ATE-ports during said testing sequence).

35 U.S.C. 103(a) rejection of claim 4.

Cheung teaches means for specifying cycle times of stimulus and response vectors for said ATE-port (col. 15, lines 16-25, Cheung);

means for specifying a pattern program for said ATE-port (see Abstract, Cheung);

means for specifying a per-pin vector data for each of said plurality of per-pin testing units assigned to said ATE-port (see Event Sequencer 24 and col.3, lines 27-40 in Cheung); and

means for specifying analogue set-up conditions for analogue pins of said ATE-port (See 12-bit DAC in Figure 6 of Cheung; Note: the Circuit in Figure 6 is the Levels Generator 62 of Figure 1).

35 U.S.C. 103(a) rejection of claim 5.

Cheung teaches main pattern programs for implementing access protocols to said first DUT core (col. 1, lines 13-37 of Cheung explicitly teach that the test system computer within an ATE stores programs for testing the DUT and the Abstract in Cheung explicitly teaches that the different groupings of pin slice circuits are programmed whereby pin slice circuits in the same group are programmed with the same test signals; Note: the programs for testing the DUT stored within the test system computer are main pattern programs for implementing access protocols to DUT core functional circuitry).

35 U.S.C. 103(a) rejection of claim 6.

Cheung teaches a means for configuring said ATE-port for activating said subset of said plurality of per-pin testing units for accessing said first DUT core (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit; the participate memory taught in the Cheung patent is a means for configuring said ATE-port for activating said subset of said plurality of per-pin testing units for accessing said first DUT core).

35 U.S.C. 103(a) rejection of claim 7.

Cheung teaches a means for specifying an alias mapping between said plurality of per-pin testing units for a plurality of ATE-ports, for specifying at least one of timing information and a pattern program of said ATE-port to apply for said plurality of ATE-ports for which said alias mapping is defined (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a

specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit; the participate memory taught in the Cheung patent is a means for specifying an alias mapping between said plurality of per-pin testing units for a plurality of ATE-port groupings, for specifying at least one of timing information and a pattern program of said ATE-port to apply for said plurality of ATE-port groupings for which said alias mapping is defined).

35 U.S.C. 103(a) rejection of claim 8.

Cheung teaches in means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit; the participate memory taught in the Cheung patent is a means for

specifying overall test conditions for a test that concurrently operates on multiple ATE-ports).

35 U.S.C. 103(a) rejection of claim 9.

Cheung teaches means for determining a set of concurrently active ATE-ports during a defined testing sequence (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit; the participate memory taught in the Cheung patent is a means for determining a set of concurrently active ATE-ports during a defined testing sequence); means for selecting ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins (the participate memory taught in the Cheung patent is a means for selecting ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins; Note: Claim 12 in Cheung teaches that Event Sequencer Memory 24 in figure 1 of Cheung stores a plurality of timing criteria for each pin, i.e., per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port;

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Note: see col. 2, lines 26-33, Cheung for additional details);

means for specifying global test conditions to express dependencies between pins of said DUT and said ATE (the participate memory taught in the Cheung patent is a means for specifying global test conditions to express dependencies between pins of said DUT and said ATE; Note: col. 3, lines 27-40 in Cheung teach a Global Sequencer for specifying global test conditions to express dependencies between pins of the DUT and the ATE); and

means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port (col. 3, lines 27-40 in Cheung teach that the Event Sequencer is a means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port).

35 U.S.C. 103(a) rejection of claim 10.

Cheung teaches a method for testing a device under test (DUT) with automated test equipment, ATE (col. 1, lines 13-14, Cheung) having:

a plurality of per-pin testing units (See Figure 1 in Cheung), wherein each of said plurality of per-pin testing units has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test (DUT) having a plurality of DUT pins (Driver 26 and Comparator 28 in Figure 1 of Cheung are circuitry providing each of said plurality of per-pin testing units circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test), said method comprising: defining for a testing sequence 1. a first DUT core that represents a first functional unit

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of said DUT and 2. a second DUT core that represents a second functional unit of said DUT (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit); assigning, during said testing sequence, a subset of said plurality of per-pin testing units to an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins (col. 2, lines 8-15 in Cheung teach that groups of Pin Slice Circuits are used to test different functional components giving an example whereby one 6 pin group is used for testing transistor-transistor logic, TTL, and another grouping of six pins is used for testing Emitter Coupled Logic, ECL, and another grouping comprising the 6 pin group for testing the TTL functional unit and the 6 pin group for testing the ECL functional unit is used to test the combined TTL-ECL functional unit; the Abstract in Cheung teaches that participate memory is a means for assigning groupings of Pin Slice Circuits; Note: the pin channels for a grouping comprise an ATE-port for the particular functional unit that is being tested, for example; the 6 pin group for testing the TTL functional unit is an ATE-port, the 6 pin group for testing the ECL functional unit is an ATE-port and the 12 pin group for testing the combined TTL-ECL functional unit is an

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ATE-port); programming said ATE-port with a program for testing said first DUT core (col. 1, lines 13-37 of Cheung explicitly teach that the test system computer within an ATE stores programs for testing the DUT and the Abstract in Cheung explicitly teaches that the different groupings of pin slice circuits are programmed whereby pin slice circuits in the same group are programmed with the same test signals), wherein said program defines at least one of programming timing or a stimulus/response pattern (see Abstract; Note: a test signal is a stimulus/response pattern), and specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port (Claim 12 in Cheung teaches that Event Sequencer Memory 24 in figure 1 of Cheung stores a plurality of timing criteria for each pin, i.e., per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port), wherein each waveform represents a sequence of events of various types occurring at specified instances in time (Event Sequencer 24 in Figure 1 of Cheung teaches each waveform represents a sequence of events of various types occurring at specified instances in time), and wherein said program is independent of a program for testing said second DUT core (col. 2, lines 8-15 of Cheung explicitly teach “one grouping from the participate memory is used to program the data pattern in parallel to the dozen inputs, while two separate groupings are used to program the voltage levels for digital zeros and ones separately for the TTL inputs and the ECL inputs”, hence Cheung teaches two different programs, a first test program for a first grouping and a second test program for second and third groupings).

However Cheung does not explicitly teach the specific use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification.

Le, in an analogous art, teaches use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification (Figure 2 and 4 in Le teaches a programming component that obtains a specification 270 in Figure 2 for testing a DUT core and prepares a program 460 in Figure 4 based on said specification 270). Note: col. 4, lines 23-33 in Cheung teach that various test programs are required to implement the design in Cheung, but does not teach the details to the test program generation. Le, on the other hand teaches test program generation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cheung with the teachings of Le by including use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification would have provided the opportunity to generate the test programs required in the Cheung patent.

35 U.S.C. 103(a) rejection of claim 12.

Cheung teaches specifying cycle times of stimulus and response vectors for said ATE-port (col. 15, lines 16-25, Cheung);
specifying a pattern program for said ATE-port (see Abstract, Cheung);
specifying a per-pin vector data for each of said plurality of per-pin testing units assigned to said ATE-port (see Event Sequencer 24 and col.3, lines 27-40 in Cheung);
and
specifying analogue set-up conditions for analogue pins of said ATE-port (See 12-bit DAC in Figure 6 of Cheung; Note: the Circuit in Figure 6 is the Levels Generator 62 of Figure 1).

35 U.S.C. 103(a) rejection of claim 13.

Cheung teaches specifying overall test conditions for a test that concurrently operates on multiple ATE-ports (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit; the participate memory taught in the Cheung patent is a means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports).

35 U.S.C. 103(a) rejection of claim 14.

Cheung teaches determining a set of concurrently active ATE-ports during a defined testing sequence (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit; the participate memory taught in the Cheung patent is a means for determining a set of concurrently active ATE-ports during a defined testing sequence); selecting ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins (the participate memory taught in the Cheung patent is a means for selecting ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins; Note: Claim 12 in Cheung teaches that Event Sequencer Memory 24 in figure 1 of Cheung stores a plurality of timing criteria for each pin, i.e., per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port; Note: see col. 2, lines 26-33, Cheung for additional details); specifying global test conditions to express dependencies between pins of said DUT

and said ATE (the participate memory taught in the Cheung patent is a means for specifying global test conditions to express dependencies between pins of said DUT and said ATE; Note: col. 3, lines 27-40 in Cheung teach a Global Sequencer for specifying global test conditions to express dependencies between pins of the DUT and the ATE); and

determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port (col. 3, lines 27-40 in Cheung teach that the Event Sequencer is a means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port).

35 U.S.C. 103(a) rejection of claim 15.

Cheung teaches data media for storing computer instructions for automated test equipment ATE (col. 1, lines 13-14, Cheung; col. 1, lines 13-37 of Cheung explicitly teach that the test system computer within an ATE stores programs for testing the DUT and the Abstract in Cheung explicitly teaches that the different groupings of pin slice circuits are programmed whereby pin slice circuits in the same group are programmed with the same test signals; Note: the test system computer within an ATE is ta media for storing computer instructions for automated test equipment ATE) comprising:
instructions for testing a DUT having a plurality of per-pin testing units (See Figure 1 in Cheung), wherein each of said plurality of per-pin testing units has circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test (DUT) having a plurality of DUT pins (Driver 26 and Comparator 28 in Figure 1 of Cheung are

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circuitry providing each of said plurality of per-pin testing units circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test), instructions for defining, during a testing sequence, said DUT is defined as 1. a first DUT core that represents a first functional unit of said DUT and 2. a second DUT core that represents a second functional unit of said DUT (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit);

instructions for assigning, during said testing sequence, a subset of said plurality of per-pin testing units to an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins (col. 2, lines 8-15 in Cheung teach that groups of Pin Slice Circuits are used to test different functional components giving an example whereby one 6 pin group is used for testing transistor-transistor logic, TTL, and another grouping of six pins is used for testing Emitter Coupled Logic, ECL, and another grouping comprising the 6 pin group for testing the TTL functional unit and the 6 pin group for testing the ECL functional unit is used to test the combined TTL-ECL functional unit; the Abstract in Cheung teaches that participate memory is a means for assigning groupings

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of Pin Slice Circuits; Note: the pin channels for a grouping comprise an ATE-port for the particular functional unit that is being tested, for example; the 6 pin group for testing the TTL functional unit is an ATE-port, the 6 pin group for testing the ECL functional unit is an ATE-port and the 12 pin group for testing the combined TTL-ECL functional unit is an ATE-port); and instructions for programming said ATE-port with a program for testing said first DUT core (col. 1, lines 13-37 of Cheung explicitly teach that the test system computer within an ATE stores programs for testing the DUT and the Abstract in Cheung explicitly teaches that the different groupings of pin slice circuits are programmed whereby pin slice circuits in the same group are programmed with the same test signals), wherein said program defines at least one of programming timing or a stimulus/response pattern (see Abstract; Note: a test signal is a stimulus/response pattern), and specifies a per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port (Claim 12 in Cheung teaches that Event Sequencer Memory 24 in figure 1 of Cheung stores a plurality of timing criteria for each pin, i.e., per-pin timing in terms of sets of available waveforms for each of said plurality of per-pin testing units assigned to said ATE-port), wherein each waveform represents a sequence of events of various types occurring at specified instances in time (Event Sequencer 24 in Figure 1 of Cheung teaches each waveform represents a sequence of events of various types occurring at specified instances in time), and wherein said program is independent of a program for testing said second DUT core (col. 2, lines 8-15 of Cheung explicitly teach "one grouping from the participate memory is used to program the data pattern in parallel to the dozen inputs,

while two separate groupings are used to program the voltage levels for digital zeros and ones separately for the TTL inputs and the ECL inputs”, hence Cheung teaches two different programs, a first test program for a first grouping and a second test program for second and third groupings).

However Cheung does not explicitly teach the specific use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification.

Le, in an analogous art, teaches use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification (Figure 2 and 4 in Le teaches a programming component that obtains a specification 270 in Figure 2 for testing a DUT core and prepares a program 460 in Figure 4 based on said specification 270). Note: col. 4, lines 23-33 in Cheung teach that various test programs are required to implement the design in Cheung, but does not teach the details to the test program generation. Le, on the other hand teaches test program generation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cheung with the teachings of Le by including use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a programming component that obtains a specification for testing said first DUT core and prepares a

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program based on said specification would have provided the opportunity to generate the test programs required in the Cheung patent.

35 U.S.C. 103(a) rejection of claim 16.

Cheung teaches automated test equipment (col. 1, lines 13-14, Cheung), comprising: a plurality of per-pin testing units (See Figure 1 in Cheung), wherein each of said plurality of per-pin testing units is configurable for at least one of emitting a stimulus signal to, or receiving a response signal from, a pin of a device under test (DUT) having a plurality of DUT pins (Driver 26 and Comparator 28 in Figure 1 of Cheung are circuitry providing each of said plurality of per-pin testing units circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test), and wherein, during a testing sequence, said DUT is defined as having a first functional unit and a second functional unit (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit); means for assigning a subset of said plurality of per-pin testing units to an ATE-port for interfacing with said first functional unit via a subset of said plurality of DUT pins (col. 2, lines 8-15 in Cheung

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teach that groups of Pin Slice Circuits are used to test different functional components giving an example whereby one 6 pin group is used for testing transistor-transistor logic, TTL, and another grouping of six pins is used for testing Emitter Coupled Logic, ECL, and another grouping comprising the 6 pin group for testing the TTL functional unit and the 6 pin group for testing the ECL functional unit is used to test the combined TTL-ECL functional unit; the Abstract in Cheung teaches that participate memory is a means for assigning groupings of Pin Slice Circuits; Note: the pin channels for a grouping comprise an ATE-port for the particular functional unit that is being tested, for example; the 6 pin group for testing the TTL functional unit is an ATE-port, the 6 pin group for testing the ECL functional unit is an ATE-port and the 12 pin group for testing the combined TTL-ECL functional unit is an ATE-port); and means for programming said ATE-port with a program for testing said first functional unit (col. 1, lines 13-37 of Cheung explicitly teach that the test system computer within an ATE stores programs for testing the DUT and the Abstract in Cheung explicitly teaches that the different groupings of pin slice circuits are programmed whereby pin slice circuits in the same group are programmed with the same test signals), wherein said program is independent of a program for testing said second functional unit (col. 2, lines 8-15 of Cheung explicitly teach "one grouping from the participate memory is used to program the data pattern in parallel to the dozen inputs, while two separate groupings are used to program the voltage levels for digital zeros and ones separately for the TTL inputs and the ECL inputs", hence Cheung teaches two different programs, a first test program for a first grouping and a second test program for second and third groupings).

However Cheung does not explicitly teach the specific use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification.

Le, in an analogous art, teaches use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification (Figure 2 and 4 in Le teaches a programming component that obtains a specification 270 in Figure 2 for testing a DUT core and prepares a program 460 in Figure 4 based on said specification 270). Note: col. 4, lines 23-33 in Cheung teach that various test programs are required to implement the design in Cheung, but does not teach the details to the test program generation. Le, on the other hand teaches test program generation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cheung with the teachings of Le by including use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification would have provided the opportunity to generate the test programs required in the Cheung patent.

35 U.S.C. 103(a) rejection of claim 17.

Cheung teaches automated test equipment (col. 1, lines 13-14, Cheung), comprising: a plurality of per-pin testing units (Driver 26 and Comparator 28 in Figure 1 of Cheung are circuitry providing each of said plurality of per-pin testing units circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test), wherein each of said plurality of per-pin testing units is configurable for at least one of emitting a stimulus signal to, or receiving a response signal from, a pin of a device under test (Driver 26 and Comparator 28 in Figure 1 of Cheung are circuitry providing each of said plurality of per-pin testing units circuitry for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test), and wherein, during a testing sequence, said DUT is defined as having a first functional unit and a second functional unit (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit); and an ATE-port that receives a program for testing said first functional unit, and interfaces with said first functional unit via a subset of said plurality of per-pin testing units (col. 1, lines 13-37 of Cheung explicitly teach that the test system computer within an ATE stores programs for testing the DUT and the Abstract in Cheung explicitly teaches that the different

groupings of pin slice circuits are programmed whereby pin slice circuits in the same group are programmed with the same test signals).

However Cheung does not explicitly teach the specific use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification.

Le, in an analogous art, teaches use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification (Figure 2 and 4 in Le teaches a programming component that obtains a specification 270 in Figure 2 for testing a DUT core and prepares a program 460 in Figure 4 based on said specification 270). Note: col. 4, lines 23-33 in Cheung teach that various test programs are required to implement the design in Cheung, but does not teach the details to the test program generation. Le, on the other hand teaches test program generation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cheung with the teachings of Le by including use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a programming component that obtains a specification for testing said first DUT core and prepares a program based on said specification would have provided the opportunity to generate the test programs required in the Cheung patent.

35 U.S.C. 103(a) rejection of claim 18.

Cheung teaches said ATE-port is a first ATE-port, and said subset is a first subset, and wherein said ATE further comprises a second ATE-port that receives a program for testing said second functional unit, and interfaces with said second functional unit via a second subset of said plurality of per-pin testing units (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit).

35 U.S.C. 103(a) rejection of claim 19.

Cheung teaches said program for testing said first functional unit is independent of said program for testing said second functional unit (The Abstract in Cheung teaches that each pin slice circuit can be independently programmed and tested, hence any test program for any grouping is independent of any other test program for any other grouping).

35 U.S.C. 103(a) rejection of claim 20.

Cheung teaches in means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports (the Abstract in Cheung teaches that a participate memory is used to select different groupings of the pin slice circuits which are to be programmed in parallel; Note: a grouping of pin slice circuits is attached to a specific group of functional core circuitry within the DUT that is accessed through the selected group of pins, hence each different grouping of pin slice circuits is attached to different functional core circuitry for testing the different functional core circuitry and each of the different functional core circuitry within the DUT that are selected by selecting different grouping of pin slice circuits represent different core functional units within the circuit; the participate memory taught in the Cheung patent is a means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports).

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

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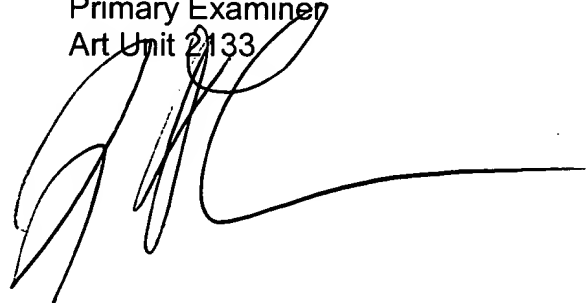
mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Joseph D. Torres, PhD
Primary Examiner
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A handwritten signature in black ink, appearing to be 'JDT', is written over the printed name and title of the examiner.